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IN THE U.S. PATENT AND TRADEMARK OFFICE
Patent Application Transmittal Letter

COMMISSIONER FOR PATENTS
Washington, D.C. 20231

J1033 U.S. PTO
09/1891324
06/27/01

Sir:

Transmitted herewith for filing under 37 CFR 1.53(b) is a(n): Utility Design

- original patent application,
 continuation-in-part application

INVENTOR(S): Osamu Samuel NAKAGAWA

TITLE: PROCESS FOR HIGH-DIELECTRIC CONSTANT METAL-INSULATOR METAL CAPICATOR IN VLSI MULTI-LEVEL METALLIZATION SYSTEMS

Enclosed are:

- The Declaration and Power of Attorney. signed unsigned or partially signed
 4 sheets of drawings (one set) Associate Power of Attorney
 Form PTO-1449 Information Disclosure Statement and Form PTO-1449
 Priority document(s) (Other) (fee \$ _____)

CLAIMS AS FILED BY OTHER THAN A SMALL ENTITY				
(1) FOR	(2) NUMBER FILED	(3) NUMBER EXTRA	(4) RATE	(5) TOTALS
TOTAL CLAIMS	19 — 20	0	X \$18	\$ 0
INDEPENDENT CLAIMS	2 — 3	0	X \$80	\$ 0
ANY MULTIPLE DEPENDENT CLAIMS	0		\$270	\$ 0
BASIC FEE: Design (\$320.00); Utility (\$710.00)				\$ 710
TOTAL FILING FEE				\$ 710
OTHER FEES				\$
TOTAL CHARGES TO DEPOSIT ACCOUNT				\$ 710

Charge \$ 710 to Deposit Account 08-2025. At any time during the pendency of this application, please charge any fees required or credit any over payment to Deposit Account 08-2025 pursuant to 37 CFR 1.25. Additionally please charge any fees to Deposit Account 08-2025 under 37 CFR 1.16, 1.17, 1.19, 1.20 and 1.21. A duplicate copy of this sheet is enclosed.

"Express Mail" label no. _____

Respectfully submitted,

Date of Deposit _____

Osamu Samuel NAKAGAWA

I hereby certify that this is being deposited with the United States Postal Service "Express Mail Post Office to Addressee" service under 37 CFR 1.10 on the date indicated above and is addressed to: Commissioner for Patents, Washington, D.C. 20231.

By _____

Typed Name:

By John W. Ryan
John W. Ryan

Attorney/Agent for Applicant(s)

Reg. No. 33,771

Date: June 24, 2001

Telephone No.: (202) 663-6446

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

UTILITY PATENT APPLICATION FOR:

**PROCESS FOR HIGH-DIELECTRIC CONSTANT METAL-
INSULATOR METAL CAPACITOR IN VLSI MULTI-LEVEL
METALLIZATION SYSTEMS**

Inventor:

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